Application Note

Document No.: AN1158

Migrate from APM32F407 to APM32F425/427

Version: V1.0

1. Introduction

For embedded system designers, it is crucial to be able to easily migrate applications between different series of microcontrollers. As product demands continue to rise, the requirements for resources such as memory size and I/O quantity also increase accordingly. Designers often need to port applications to microcontrollers with higher performance or more resources.

This transplantation manual is intended to help users analyze from existing APM32F407 device the steps required to migrate to APM32F425/427 device. This document collects the most important information and lists the key matters that need attention during the migration process. The main aspects involved in the migration process include hardware transplantation, peripheral transplantation, firmware transplantation and toolchain transplantation.

In order to make full use of the information in this manual, the user should be familiar with the features of APM32F427 series microcontroller and development environment. You can refer to the following relevant technical documents

- APM32F425/427 series user manuals and data sheet
- APM32F425/427 series core document

1.1. Introduction

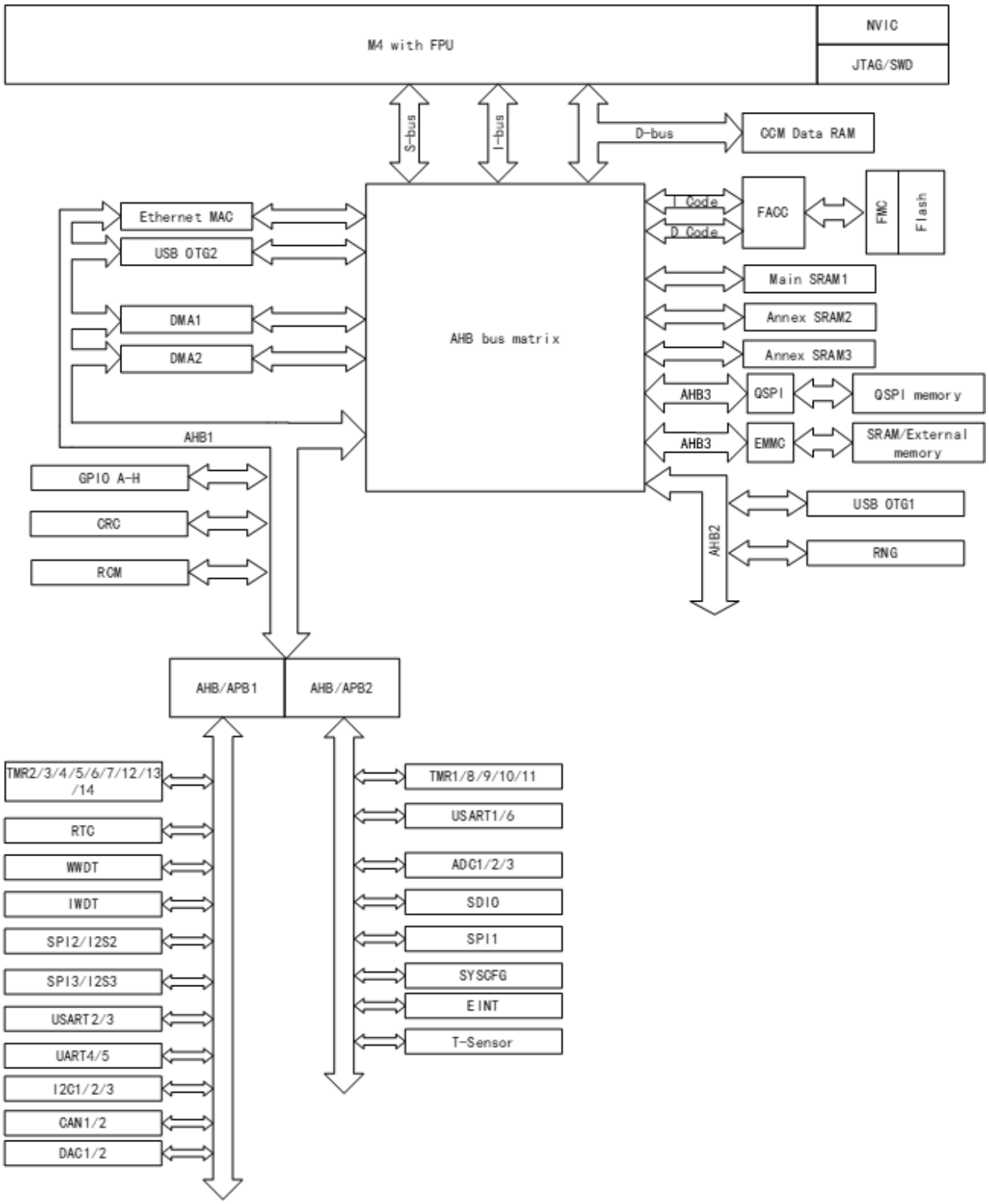
The Arm® Cortex®-M4F core in the product is equipped with an FPU. The system is mainly composed of one master module and eight slave modules.

The main modules are respectively I-bus, D-bus and S-bus general-purpose DMA1, general-purpose DMA2 with Arm® Cortex®-M4F cores featuring FPU, Ethernet DMA bus and USB OTG bus.

The slave modules are the I-bus and D-bus of the internal Flash, the main internal memory SRAM1, the auxiliary internal memory SRAM2 and SRAM3 (only supported by APM32F427), and all peripheral devices connected by the AHB1 bus and the AHB1/APB bridge. Peripherals on the AHB2 bus and QSPI and EMMC on the AHB3 bus.

APM32F425/427 architecture is shown in figure 1.

Figure 1 APM32F425/427 system architecture



目录

2. Hardware Migration

2.1. Pin Arrangement

The pins of APM32F425/427 are compatible with those of the corresponding packages of the APM32F407 series, making migration and replacement extremely convenient.

Table 1 All series package

package	APM32F407	APM32F425/427	compatibility
QFN48	NA	Y	/
LQFP48	NA	Y	/
LQFP64	Y	Y	Pin compatibility except for I2S, OTG_HS, DCI, and DMC
LQFP100	Y	Y	Pin compatibility except for I2S, OTG_HS, DCI, and DMC
LQFP144	Y	Y	Pin compatibility except for I2S, OTG_HS, DCI, and DMC

Note: Y indicates that this series of chips has the corresponding package.

2.2. Boot Configure

The BOOT mode entry method of APM32F425/427 is the same as that of APM32F407. By configuring the BOOT[1:0] pin parameter, three different boot modes can be switched.

2.3. Built-in Bootloader

The specific differences in the built-in bootloaders between APM32F425/427 and APM32F407 are shown in the table below.

Table 2 Bootloader correlation table

Bootloader mode	APM32F407	APM32F425/427
USART1	Y	Y
USART3	Y	Y
CAN2	Y	Y
USB OTG FS slave device mode	Y	Y
I2C1	NA	Y

Note:

1. Y indicates that this series of chips has the corresponding mode.
2. When operating the Bootloader using the USB DFU or CAN protocol, the oscillator frequency (HSECLK) range of the external high-speed crystal oscillator (HSE) is limited to 4 to 16MHz.

3. Software Mobility

Compared with APM32F407, the peripheral part of APM32F425/427 has simplified peripherals such as DCI, I2S, and USB OTG HS, and also added a QSPI peripheral. For these peripherals, they need to be modified in the application layer program development or newly developed by referring to the standard firmware library of APM32F425/427.

3.1. Peripheral resources comparison

To clearly demonstrate the differences in peripheral resources between APM32F425/427 and APM32F407, the following table takes the largest package of APM32F425/427 as the benchmark to compare the main peripheral resources of these two microcontrollers.

Table 3 APM32F425/427 and APM32F407 peripheral resource comparison table

Product		APM32F425/427	APM32F407
Core and maximum working frequency		Arm® 32-bit Cortex®-M4F@240MHz	Arm® 32-bit Cortex®-M4F@168MHz
Flash(KB)		1024	1024
SRAM(KB)		448（F427）/ 192（F425）	192
SMC		1	1
DMC		1	1
Communication interface	USART/UART	4/2	4/2
	SPI/I2S	3/0	3/2
	I2C	3	3
	USB OTG FS	2	1
	USB OTG HS1	0	1
	USB OTG HS2	0	1
	CAN	2	2
	ETH	1	1
	QSPI	1	0
	SDIO	1	1
Timer	16-bit advanced	2	2
	32-bit general	4	2
	16-bit general	6	8
	16-bit basic	2	2
	System tick timer	1	1
	Watchdog	2	2
Real-time clock		1	1
DCI		0	1
12-bit ADC	Unit / Channel	3/21	3/24

12 bit DAC	**Unit / Channel**	2/2	2/2

3.2. CPU Core

Both APM32F425/427 and APM32F407 are based on the Arm® Cortex®-M4F core and support an additional FPU, enabling them to perform floating-point operations efficiently.

3.3. Interrupt Vector Table Difference

The maximum interrupt number supported by APM32F425/427 is 66, and all interrupts are given to the CPU through the Nested Vector Interrupt Controller (NVIC). The External Interrupt Controller (EINT) provides external interrupts (GPIO).

Table 4 Interrupted and abnormal functions comparison

function	APM32F425/427	APM32F407
Interrupt number	79	84
Interrupt priority (bit)	4	4

On the interrupt vector table, APM32F425/427 and APM32F407 are not the same. The differences between the two can be referred to in the following table.

Table 5 Interrupt vector comparison table

Vector ID	APM32F425/427	APM32F407
0	WWDT	WWDT
1	PVD	PVD
2	TAMP_STAMP	TAMP_STAMP
3	RTC_WKUP	RTC_WKUP
4	FLASH	FLASH
5	RCM	RCM
6	EINT0	EINT0
7	EINT1	EINT1
8	EINT2	EINT2
9	EINT3	EINT3
10	EINT4	EINT4
11	DMA1_STR0	DMA1_STR0
12	DMA1_STR1	DMA1_STR1
13	DMA1_STR2	DMA1_STR2
14	DMA1_STR3	DMA1_STR3
15	DMA1_STR4	DMA1_STR4

Vector ID	APM32F425/427	APM32F407
16	DMA1_STR5	DMA1_STR5
17	DMA1_STR6	DMA1_STR6
18	ADC	ADC
19	CAN1 TX	CAN1 TX
20	CAN1 RX0	CAN1 RX0
21	CAN1 RX1	CAN1 RX1
22	CAN1 SCE	CAN1 SCE
23	EINT9_5	EINT9_5
24	TMR1_BRK_TMR9	TMR1_BRK_TMR9
25	TMR1_UP_TMR10	TMR1_UP_TMR10
26	TMR1_TRG_COM_TMR11	TMR1_TRG_COM_TMR11
27	TMR1_CC	TMR1_CC
28	TMR2	TMR2
29	TMR3	TMR3
30	TMR4	TMR4
31	I2C1_EV	I2C1_EV
32	I2C1_ER	I2C1_ER
33	I2C2_EV	I2C2_EV
34	I2C2_ER	I2C2_ER
35	SPI1	SPI1
36	SPI2	SPI2
37	USART1	USART1
38	USART2	USART2
39	USART3	USART3
40	EINT15_10	EINT15_10
41	RTC_Alarm	RTC_Alarm
42	OTG_FS WKUP	OTG_FS WKUP
43	TMR8_BRK_TMR12	TMR8_BRK_TMR12
44	TMR8_UP_TMR13	TMR8_UP_TMR13
45	TMR8_TRG_COM_TMR14	TMR8_TRG_COM_TMR14
46	TMR8 CC	TMR8 CC
47	DMA1_STR7	DMA1_STR7

Vector ID	APM32F425/427	APM32F407
48	EMMC	EMMC
49	SDIO	SDIO
50	TMR5	TMR5
51	SPI3	SPI3
52	UART4	UART4
53	UART5	UART5
54	TMR6_DAC	TMR6_DAC
55	TMR7	TMR7
56	DMA2_STR0	DMA2_STR0
57	DMA2_STR1	DMA2_STR1
58	DMA2_STR2	DMA2_STR2
59	DMA2_STR3	DMA2_STR3
60	DMA2_STR4	DMA2_STR4
61	ETH	ETH
62	ETH_WKUP	ETH_WKUP
63	CAN2_TX	CAN2_TX
64	CAN2_RX0	CAN2_RX0
65	CAN2_RX1	CAN2_RX1
66	CAN2_SCE	CAN2_SCE
67	OTG_FS	OTG_FS
68	DMA2_STR5	DMA2_STR5
69	DMA2_STR6	DMA2_STR6
70	DMA2_STR7	DMA2_STR7
71	USART6	USART6
72	I2C3_EV	I2C3_EV
73	I2C3_ER	I2C3_ER
74	**Reserved**	**OTG_HS1_EP1_OUT**
75	**Reserved**	**OTG_HS1_EP1_IN**
76	**Reserved**	**OTG_HS1_WKUP**
77	**Reserved**	**OTG_HS1**
78	**Reserved**	**DCI**
79	Reserved	Reserved

Vector ID	APM32F425/427	APM32F407
80	RNG	RNG
81	FPU	FPU
82	**Reserved**	**SM3**
83	**Reserved**	**SM4**
84	**Reserved**	**BN**
85	**OTG_FS2 WKUP**	**Reserved**
86	**OTG_FS2**	**Reserved**
87	**QSPI**	**Reserved**

Note: Due to the differences in interrupt vectors, if the migration involves different interrupts, please note to use the APM32F427 startup file (startup_apm32f427xx.s) of the APM32F4xx SDK V1.5.0 version.

3.4. Memory Map

The memory mapping of APM32F425/427 is shown in the following table.

Table 6 APM32F425/427 and APM32F407 memory map contrast

peripheral	APM32F425/427		APM32F407	
	bus	start address	bus	start address
TMR2	APB1	0x4000 0000	APB1	0x4000 0000
TMR3	APB1	0x4000 0400	APB1	0x4000 0400
TMR4	APB1	0x4000 0800	APB1	0x4000 0800
TMR5	APB1	0x4000 0C00	APB1	0x4000 0C00
TMR6	APB1	0x4000 1000	APB1	0x4000 1000
TMR7	APB1	0x4000 1400	APB1	0x4000 1400
TMR12	APB1	0x4000 1800	APB1	0x4000 1800
TMR13	APB1	0x4000 1C00	APB1	0x4000 1C00
TMR14	APB1	0x4000 2000	APB1	0x4000 2000
RTC	APB1	0x4000 2800	APB1	0x4000 2800
WWDT	APB1	0x4000 2C00	APB1	0x4000 2C00
IWDT	APB1	0x4000 3000	APB1	0x4000 3000
I2S2ext	**-**	**-**	**APB1**	**0x4000 3400**
SPI2	APB1	0x4000 3800	APB1	0x4000 3800
SPI3	APB1	0x4000 3C00	APB1	0x4000 3C00
I2S3ext	**-**	**-**	**APB1**	**0x4000 4000**
USART2	APB1	0x4000 4400	APB1	0x4000 4400

peripheral	APM32F425/427		APM32F407	
	bus	start address	bus	start address
USART3	APB1	0x4000 4800	APB1	0x4000 4800
UART4	APB1	0x4000 4C00	APB1	0x4000 4C00
UART5	APB1	0x4000 5000	APB1	0x4000 5000
I2C1	APB1	0x4000 5400	APB1	0x4000 5400
I2C2	APB1	0x4000 5800	APB1	0x4000 5800
I2C3	APB1	0x4000 5C00	APB1	0x4000 5C00
CAN1	APB1	0x4000 6400	APB1	0x4000 6400
CAN2	APB1	0x4000 6800	APB1	0x4000 6800
PMU	APB1	0x4000 7000	APB1	0x4000 7000
DAC	APB1	0x4000 7400	APB1	0x4000 7400
TMR1	APB2	0x4001 0000	APB**2**	0x4001 0000
TMR8	APB2	0x4001 0400	APB**2**	0x4001 0400
USART1	APB2	0x4001 1000	APB2	0x4001 1000
USART6	APB2	0x4001 1400	APB2	0x4001 1400
ADC1/2/3	APB2	0x4001 2000	APB2	0x4001 2000
SDIO	APB2	0x4001 2C00	APB2	0x4001 2C00
SPI1	APB2	0x4001 3000	APB2	0x4001 3000
SYSCFG	APB2	0x4001 3800	APB**2**	0x4001 3800
EINT	APB2	0x4001 3C00	APB**2**	0x4001 3C00
TMR9	APB2	0x4001 4000	APB**2**	0x4001 4000
TMR10	APB2	0x4001 4400	APB**2**	0x4001 4400
TMR11	APB2	0x4001 4800	APB**2**	0x4001 4800
GPIOA	AHB	0x4002 0000	AHB	0x4002 0000
GPIOB	AHB	0x4002 0400	AHB	0x4002 0400
GPIOC	AHB	0x4002 0800	AHB	0x4002 0800
GPIOD	AHB	0x4002 0C00	AHB	0x4002 0C00
GPIOE	AHB	0x4002 1000	AHB	0x4002 1000
GPIOF	AHB	0x4002 1400	AHB	0x4002 1400
GPIOG	AHB	0x4002 1800	AHB	0x4002 1800
GPIOH	AHB	0x4002 1C00	AHB	0x4002 1C00
GPIOI	-	-	**AHB**	**0x4002 2000**

peripheral	APM32F425/427		APM32F407	
	bus	start address	bus	start address
CRC	AHB	0x4002 3000	AHB	0x4002 3000
RCM	AHB	0x4002 3800	AHB	0x4002 3800
FMC Reg	AHB	0x4002 3C00	AHB	0x4002 3C00
back-up SRAM	AHB	0x4002 4000	AHB	0x4002 4000
DMA1	AHB	0x4002 6000	AHB	0x4002 6000
DMA2	AHB	0x4002 6400	AHB	0x4002 6400
MAC	AHB	0x4002 8000	AHB	0x4002 8000
USB OTG_HS1/2	**-**	**-**	**AHB**	**0x4004 0000**
USB OTG FS2	**AHB**	**0x4004 0000**	**-**	**-**
OTG_FS	AHB	0x5000 0000	AHB	0x5000 0000
DCI	**-**	**-**	**AHB**	**0x5005 0000**
RNG	AHB	0x5006 0800	AHB	0x5006 0800
SM4	**-**	**-**	**AHB**	**0x5008 0000**
SM3	**--**	**-**	**AHB**	**0x5008 0400**
BN	**-**	**-**	**AHB**	**0x500A 0000**
EMMC bank 1	AHB	0x6000 0000	AHB	0x6000 0000
EMMC bank 1	AHB	0x6400 0000	AHB	0x6400 0000
EMMC bank 1	AHB	0x6800 0000	AHB	0x6800 0000
EMMC bank 1	AHB	0x6C00 0000	AHB	0x6C00 0000
EMMC bank 2	AHB	0x7000 0000	AHB	0x7000 0000
EMMC bank 3	AHB	0x8000 0000	AHB	0x8000 0000
PCCARD	AHB	0x9000 0000	AHB	0x9000 0000
QSPI	**AHB**	**0x9000 0000**	**-**	**-**
EMMC Reg	AHB	0xA000 0000	AHB	0xA000 0000
QSPI Reg	**AHB**	**0xA000 1000**	**-**	**-**

3.5. Clock tree difference

The clock usage of APM32F425/427 is similar to that of APM32F407, but there are also some differences in the clocks. The differences are shown in the following table.

Table 7 Clock structure comparison table

Clock	APM32F425/427	APM32F407
LSICLK	support	support

LSECLK	support	support
HSICLK	support	support
HSECLK	support	support
RTCCLK	support	support
SMCCLK	support	support
DMCCLK	support	support
SYSCLK	support	support
HCLK	support	support
FCLK	support	support
PCLK1	support	support
PCLK2	support	support
PLLCLK	support	support
PLL2CLK	Not supported	support
I2SCLK	Not supported	support
TMRxCLK	support	support
ADCCLK	support	support
MACTXCLK	support	support
MACRXCLK	support	support
MACRMIICLK	support	support
I2SxCLK	Not supported	support

3.7. Functional Difference

This chapter describes the differences in peripheral functions between the APM32F425/427 and APM32F407 series.

Table 8 APM32F425/427 and APM32F407 peripherals compatibility table

peripheral	APM32F425/427	APM32F407	pin configuration	Firmware Drivers
ADC	Y+	Y	same	compatibility
CAN	Y	Y	same	compatibility
CRC	Y	Y	-	compatibility
DBGMCU	Y	Y	-	compatibility
DMA	Y	Y	-	compatibility
DAC	Y	Y	same	compatibility
DMC	Y+	Y	disaffinity	compatibility
EINT	Y	Y	same	compatibility
ETH	Y	Y	same	compatibility
FMC	Y+	Y	-	compatibility
GPIO	Y	Y	same	compatibility
I2C	Y	Y	same	compatibility
I2S	NA	Y	NA	NA
IWDT	Y	Y	-	compatibility
PMU	Y	Y	-	compatibility
QSPI	Y	NA	NA	NA
RCM	Y+	Y	same	compatibility
RNG	Y	Y	-	compatibility
RTC	Y	Y	same	compatibility
SPI	Y	Y	same	compatibility
SDIO	Y	Y	same	compatibility
SMC	Y	Y	same	compatibility
SYSCFG	Y	Y	-	compatibility
TMR	Y+	Y	same	compatibility
USART	Y	Y	same	compatibility
OTG FS	Y	Y	same	compatibility
OTG FS2	Y	NA	NA	NA
OTG HS1	NA	Y	NA	NA

peripheral	APM32F425/427	APM32F407	pin configuration	Firmware Drivers
OTG HS2	NA	Y	NA	NA
WWDT	Y	Y	-	compatibility

Note:

1. Y indicates that this series of chips has corresponding peripherals.
2. Y+ indicates that there are relatively new functional features.

3.7.1. GPIO 5V tolerance pin compatibility

The APM32F425/427 offers more 5V voltage input tolerance pins compared to the APM32F407. All IO type pins except the power and reset pins have the 5V voltage input tolerance feature.

3.7.2. ADC module

The sampling rate of the APM32F425/427 ADC module at 12-bit has been increased to 4MSPS, and a new oversampling control (register ADC_OSAMPCTRL) has been added.

Compared with APM32F407, APM32F425/427 provides more apis to support the use of new ADC features. For details, please refer to the table below.

Table 9 The APM32F425/427 ADC module has added a new function API

NO.	API	function
1	ADC_EnableOverSampling	enable oversampling mode
2	ADC_DisableOverSampling	disable oversampling mode
3	ADC_ConfigOverSamplingRatio	configure oversampling rate
4	ADC_ConfigOverSamplingShift	configure oversampling shift
5	ADC_ConfigOverSamplingTrigger	configure oversampling trigger

3.7.3. DMC module

The APM32F425/427 DMC module has modified the configuration of the data width (register DMC_CFG[14:13]). 0x00 indicates that the SDRAM data bit width is configured as 8bits, and 0x01 indicates that the SDRAM data bit width is configured as 16bits. The RD delay clock configuration bits (DMC_CTRL2[4:2] and DMC_CTRL2[11:10]) have been extended.

3.7.4. I2S module

The APM32F425/427 does not have an I2S module.

3.7.5. QSPI module

The APM32F425/427 has added a QSPI module, integrating a FIFO for both transmission and

reception. It features four transmission modes, supports data frame size transmission between 4-bit and 32-bit, and enables control of chip selection signal lines through either hardware or software. In four-wire transmission mode, it supports clock extension, variable instruction length, address length, waiting period, data frame size, and programmable delay of sampling time when receiving serial data, which can achieve a higher serial data bit sampling ratio.

3.7.6. RCM module

The maximum frequency of APM32F425/427 is up to 240MHz, and it has added a QSPI module, an OTG FS2 instance, and removed the OTG HS1, OTG HS2 and I2S modules. Therefore, in the RCM module, the QSPI clock enable configuration (register RCM_AHB3CLK[1]), QSPI clock reset configuration (register RCM_AHB3RST[1]), OTG FS2 clock enable configuration (register RCM_AHB1CLKEN[29]), and OTG have been added FS2 clock reset configuration (register RCM_AHB1RST[29]) and removal of PLL2-related configuration (register RCM_PLL2CFG).

3.7.7. Flash zero-wait

Compared with APM32F407, APM32F425 adds the feature of Flash zero wait. After the chip starts up, it defaults to moving the first 256KB of Flash code to 256KB SRAM3 for operation, achieving a zero-wait effect. Users should be aware that code larger than 256KB does not have a zero-wait effect, and in APM32F425, SRAM3 cannot be used as regular SRAM.

3.7.8. FMC module

The Flash of APM32F425/427 adds read break and prefetch policy control compared with APM32F407, and the configurable range of the waiting period is also larger. The following table is a comparison of the Flash functions between APM32F425/427 and APM32F407.

Table 10 Flash Functions between APM32F425/427 and APM32F407 comparison table

function	APM32F425/427	APM32F407
capacity	maximum 1024KB	maximum 1024KB
Flash wait cycle	**0 (0 < SYSCLK ≤ 30)**	**0 (0 < SYSCLK ≤ 30)**
	1 (30 < SYSCLK ≤ 60)	**1 (30 < SYSCLK ≤ 60)**
	2 (60 < SYSCLK ≤ 90)	**2 (60 < SYSCLK ≤ 90)**
	3 (90 < SYSCLK ≤ 120)	**3 (90 < SYSCLK ≤ 120)**
	4(120 < SYSCLK ≤ 150)	**4(120 < SYSCLK ≤ 150)**
	5(150 < SYSCLK ≤ 180)	**5(150 < SYSCLK ≤ 180)**
	6(180 < SYSCLK ≤ 210)	**NA**

function	APM32F425/427	APM32F407
	7(210 < SYSCLK ≤ 240)	NA
	…	NA
	127	NA
Prefetch policy control	support	not support
Read interrupt control	support	not support
Read interrupt time control	support	not support

Compared with APM32F407, APM32F425/427 provides more apis to support the use of new features of FMC. For details, please refer to the table below.

Table 11 APM32F425/427 FMC module has added a new function API

NO.	API	function
1	FMC_EnablePrefetch	enable prefetching policy control
2	FMC_DisablePrefetch	disable prefetching policy control
3	FMC_EnableReadInterrupt	enable read interrupt
4	FMC_DisableReadInterrupt	disable read interrupt
5	FMC_ConfigTrcMode	set the read interruption time control

3.7.9. TMR module

The resolution of the TMR3 and TMR4 counters in APM32F425/427 has been increased to 32 bits compared with APM32F407. The internal trigger remapping function of TMR2 removes OTG_HS1 SOF and replaces it with OTG_FS2 SOF (register TMR2_OPT[10]).

3.7.10. USB OTG module

Compared with APM32F407, the APM32F425/427 USB module removes OTG HS1 and OTG HS2 and adds an OTG FS2. The IP of the OTG FS2 module is the same as that of the OTG FS, with only differences in the bus address, interrupt vector, etc., as shown in the following table.

Table 12 APM32F425/427 USB OTG FS2 module

project	message
bus address	0x4004 0000
Global interrupt vector	86
Wake up interrupt vector	85

4. Version History

Table 13 Document Version History

Date	Version	Change History
June,2025	1.0	New

Statement

This document is formulated and published by Geehy Semiconductor Co., Ltd. (hereinafter referred to as “Geehy”). The contents in this document are protected by laws and regulations of trademark, copyright and software copyright. Geehy reserves the right to make corrections and modifications to this document at any time. Read this document carefully before using Geehy products. Once you use the Geehy product, it means that you (hereinafter referred to as the “users”) have known and accepted all the contents of this document. Users shall use the Geehy product in accordance with relevant laws and regulations and the requirements of this document.

1. Ownership

This document can only be used in connection with the corresponding chip products or software products provided by Geehy. Without the prior permission of Geehy, no unit or individual may copy, transcribe, modify, edit or disseminate all or part of the contents of this document for any reason or in any form.

The “极海” or “Geehy” words or graphics with “®” or “™” in this document are trademarks of Geehy. Other product or service names displayed on Geehy products are the property of their respective owners.

2. No Intellectual Property License

Geehy owns all rights, ownership and intellectual property rights involved in this document.

Geehy shall not be deemed to grant the license or right of any intellectual property to users explicitly or implicitly due to the sale or distribution of Geehy products or this document.

If any third party’s products, services or intellectual property are involved in this document, it shall not be deemed that Geehy authorizes users to use the aforesaid third party’s products, services or intellectual property. Any information regarding the application of the product, Geehy hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party, unless otherwise agreed in sales order or sales contract.

3. Version Update

Users can obtain the latest document of the corresponding models when ordering Geehy products.

If the contents in this document are inconsistent with Geehy products, the agreement in the sales order or the sales contract shall prevail.

4. Information Reliability

The relevant data in this document are obtained from batch test by Geehy Laboratory or cooperative third-party testing organization. However, clerical errors in correction or errors caused by differences in testing environment may occur inevitably. Therefore, users should understand that Geehy does not bear any responsibility for such errors that may occur in this document. The relevant data in this document are only used to guide users as performance parameter reference and do not constitute Geehy's guarantee for any product performance.

Users shall select appropriate Geehy products according to their own needs, and effectively verify and test the applicability of Geehy products to confirm that Geehy products meet their own needs, corresponding standards, safety or other reliability requirements. If losses are caused to users due to user's failure to fully verify and test Geehy products, Geehy will not bear any responsibility.

5. Legality

USERS SHALL ABIDE BY ALL APPLICABLE LOCAL LAWS AND REGULATIONS WHEN USING THIS DOCUMENT AND THE MATCHING GEEHY PRODUCTS. USERS SHALL UNDERSTAND THAT THE PRODUCTS MAY BE RESTRICTED BY THE EXPORT, RE-EXPORT OR OTHER LAWS OF THE COUNTRIES OF THE PRODUCTS SUPPLIERS, GEEHY, GEEHY DISTRIBUTORS AND USERS. USERS (ON BEHALF OR ITSELF, SUBSIDIARIES AND AFFILIATED ENTERPRISES) SHALL AGREE AND PROMISE TO ABIDE BY ALL APPLICABLE LAWS AND REGULATIONS ON THE EXPORT AND RE-EXPORT OF GEEHY PRODUCTS AND/OR TECHNOLOGIES AND DIRECT PRODUCTS.

6. Disclaimer of Warranty

THIS DOCUMENT IS PROVIDED BY GEEHY "AS IS" AND THERE IS NO WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, TO THE EXTENT PERMITTED BY APPLICABLE LAW.

GEEHY'S PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED FOR USE AS CRITICAL COMPONENTS IN MILITARY, LIFE-SUPPORT, POLLUTION CONTROL, OR HAZARDOUS SUBSTANCES MANAGEMENT SYSTEMS, NOR WHERE FAILURE COULD RESULT IN INJURY, DEATH, PROPERTY OR ENVIRONMENTAL DAMAGE.

IF THE PRODUCT IS NOT LABELED AS "AUTOMOTIVE GRADE," IT SHOULD NOT BE CONSIDERED SUITABLE FOR AUTOMOTIVE APPLICATIONS. GEEHY ASSUMES NO LIABILITY FOR THE USE BEYOND ITS SPECIFICATIONS OR GUIDELINES.

THE USER SHOULD ENSURE THAT THE APPLICATION OF THE PRODUCTS COMPLIES WITH ALL RELEVANT STANDARDS, INCLUDING BUT NOT LIMITED TO SAFETY, INFORMATION SECURITY, AND ENVIRONMENTAL REQUIREMENTS. THE USER ASSUMES FULL RESPONSIBILITY FOR THE SELECTION AND USE OF GEEHY PRODUCTS. GEEHY WILL BEAR NO RESPONSIBILITY FOR ANY DISPUTES ARISING FROM THE SUBSEQUENT DESIGN OR USE BY USERS.

7. Limitation of Liability

IN NO EVENT, UNLESS REQUIRED BY APPLICABLE LAW OR AGREED TO IN WRITING WILL GEEHY OR ANY OTHER PARTY WHO PROVIDES THE DOCUMENT AND PRODUCTS "AS IS", BE LIABLE FOR DAMAGES, INCLUDING ANY GENERAL, SPECIAL, DIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OR INABILITY TO USE THE DOCUMENT AND PRODUCTS (INCLUDING BUT NOT LIMITED TO LOSSES OF DATA OR DATA BEING RENDERED INACCURATE OR LOSSES SUSTAINED BY USERS OR THIRD PARTIES). THIS COVERS POTENTIAL DAMAGES TO PERSONAL SAFETY, PROPERTY, OR THE ENVIRONMENT, FOR WHICH GEEHY WILL NOT BE RESPONSIBLE.

8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.